

### **REMARKS/ARGUMENTS**

Claims 1-31 are pending in this application. Claims 1, 10, 19 and 25 are independent claims. Claims 1 and 10 have been currently amended. Claims 4, 13 and 19-31 have been withdrawn from consideration. Support for the amendment may be found throughout the Specification and drawings, especially in paragraphs [0012] and [0013] at pages 5-6 of the Specification and FIG. 2.

Claim 1 recites an element of “measuring idle time of said Serial ATA interface with a power down counter ... wherein an input clock counter counts an input clock and checks against a programmable value to generate a required frequency to operate said power down counter, said programmable value being held by a programmable register” (emphasis added). Applicants respectfully submit that the element is not taught, disclosed or suggested by Applicants Admitted Prior Art (AAPA) in view of Cortopassi et al. (“Cortopassi”, U.S. Patent No. 5,974,558).

At least based on this reason, the rejection of Claim 1 should be withdrawn and Claim 1 is allowable.

Claims 2-3 and 5-9 depend from Claim 1 and are therefore allowable due to their dependence.

Claims 10-12 and 14-18 were rejected based on the same rationales as applied to Claims 1-3 and 5-9. Thus, Claims 10-12 and 14-18 are allowable since Claims 1-3 and 5-9 are allowable.

**CONCLUSION**

In light of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in the case.

Respectfully submitted on behalf of  
LSI Logic Corporation,

Dated: August 9, 2005

By: \_\_\_\_\_

Peng Zhu

Reg. No. 48,063

SUITER • WEST PC LLO  
14301 FNB Parkway, Suite 220  
Omaha, NE 68154  
(402) 496-0300      telephone  
(402) 496-0333      facsimile